South European Test Seminar

2019

St. Leonhard, Pitztal, Austria
March 11 – 15, 2019

Organized by

Computer Engineering Group

University of Paderborn, Germany

Monday, March 11

19:00   Opening Remarks: Sybille Hellebrand, University of Paderborn

20:00   Welcome Dinner

Tuesday, March 12

Session 1: Security

Moderator: Chang Liu, University of Stuttgart

AutoFault: Towards Automatic Construction of Algebraic Fault Attacks
Tobias Paxian, University of Freiburg

Rabii-Keren Error Correcting Architectures for Cryptographic Circuits
Maël Gay, University of Stuttgart

Towards Identifying Critical Delay Faults
Devanshi Upadhyaya, University of Stuttgart

Session 2: New Strategies in Verification and Test

Moderator: Bernd Becker, University of Freiburg

Design and Verification of Heterogeneous Systems Using Constrained Random Techniques
Muhammad Hassan, University of Bremen

IC3 Meets Testing - A Case Study
Felix Winterer, University of Freiburg

Session 3: Reconfigurable Scan Networks

Moderator: Rolf Drechsler, University of Bremen

Multi-Level Simulation of Reconfigurable Scan Networks
Ahmed Atteya, University of Stuttgart

On Secure Data Flow in Reconfigurable Scan Networks
Pascal Raiola, University of Freiburg

Secureness Preserving Integration of Reconfigurable Scan Networks
Natalia Lylina, University of Stuttgart

Wednesday, March 13

Session 4: Aging and Fault Tolerance

Moderator: Sybille Hellebrand, University of Paderborn

Exploring Hardware Vulnerability against High Temperatures and Aging Mechanisms
Frank Sill Torres, University of Bremen

Programmable Delay Monitors for Small Delay Fault Testing and Aging Prediction
Chang Liu, University of Stuttgart

STAHL: A Novel Scan-Test-Aware Hardened Latch Design
Ruijun Ma, Kyushu Institute of Technology

Session 5: Analog and RF Test

Moderator: Hans-Joachim Wunderlich, University of Stuttgart

Test of 2.4 GHz ZigBee Transmitter using Standard Digital ATE
Thibault Vayssade, LIRMM Montpellier

The Use of Ensemble Learning in Indirect Testing of Analog and RF Integrated Circuits
Hassan El Badawi, LIRMM Montpellier

Session 6: Simulation and Detection of Small Delay Faults

Moderator: Ilia Polian, University of Stuttgart

GPU-accelerated Time Simulation with Statistical Learning-Based Parametric Delay Modeling
Eric Schneider, University of Stuttgart

Supply Voltage Impact on Small Delay Fault Detection
Zahra Paria Najafi Haghi, University of Stuttgart

Towards Faster-than-at-Speed Logic BIST
Matthias Kampmann, University of Paderborn

Thursday, March 14

Session 7: Compaction and Diagnosis for Small Delay Faults

Moderator: Mehdi Tahoori, Karlsruhe Institute of Technology

Small Delay Fault Diagnosis with Compacted Responses
Stefan Holst, Kyushu Institute of Technology

Divide and Compact - Stochastic Space Compaction for FAST
Alexander Sprenger, University of Paderborn

Hybrid Space Compactor for Varying X-Rates in FAST
Mohammad Urf Maaz, University of Paderborn

Session 8: Security in FPGAs

Moderator: Frank Sill Torres, University of Bremen

(ReCo)Fuse Your PRC or Loose Security: Finally Reliable Reconfiguration-Based Countermeasures on FPGAs
Buse Ustaoglu, University of Bremen

Mitigating Electrical-Level Attacks on Multi-Tenant FPGAs
Jonas Krautter, Karlsruhe Institute of Technology

Session 9: Quantum and Neuromorphic Computing

Moderator: Stefan Holst, Kyushu Institute of Technology

SAT-Based Error Propagation Analysis for Error-Corrected Quantum Computers
Sebastian Brandhofer, University of Stuttgart

Defect Implications of MTJ Crossbars for Binary Neural Networks
Christopher Münch, Karlsruhe Institute of Technology

Friday, March 15

Closing Remarks: Sybille Hellebrand, University of Paderborn